MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2019/2020 SESSION

ECE 3226 - ADVANCED COMPUTER ARCHITECTURE AND PARALLEL COMPUTING

(CE)

2 MARCH 2020
09:00 A.M – 11:00 A.M
(2 Hours)

INSTRUCTIONS TO STUDENT

1. This question paper consists of five (5) pages only (including this page).
2. There are **FOUR (4) QUESTIONS** in this paper. Answer **ALL QUESTIONS**. All questions carry 25 marks each.
3. Write your answers in the Answer Booklet provided.

Question 1

a) Parallel systems deal with the simultaneous use of multiple computer resources that can include a single computer with multiple processors. Parallel systems are more difficult to program than computers with a single processor because the architecture of parallel computers varies accordingly and the processes of multiple CPUs must be coordinated and synchronized. Compare and elaborate the main characteristics of SISD and MISD with the aid of diagrams.

[8 marks]

b) Spatial and temporal locality describe two different characteristics of how programs access data (or instructions). As a computer architect, briefly explain the differences in the characteristics between temporal locality and spatial locality in your own words.

[4 marks]

c) Computer A which has a 8GHz clock requires 10 seconds to run a particular program. As a computer engineer, you are requested to build a computer, B, which can complete this program in 6 seconds. This requires a substantial increase in the clock rate, but this increase will affect the rest of processing unit design, causing computer B to require 1.5 times as many clock cycles as computer A for this program.

i. Estimate number of CPU clock cycles for computer A

[5 marks]

ii. Estimate the clock rate for computer B

[5 marks]

d) Cache memory is a basic need generated by the fact that high processor speed can only be utilized if it can access data and instruction in memory quickly enough. Normal memory speed has not kept pace with that of processors and optimization could assist in efficiency of cache usage. In your own words, specify three types of basic cache optimization techniques.

[3 marks]

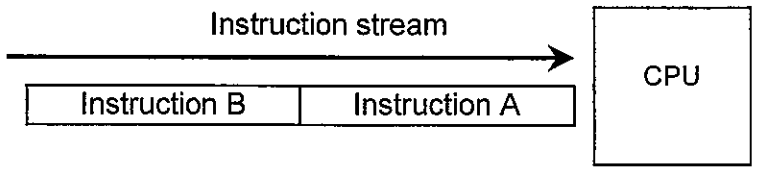
Continued .....

Question 2

a) The architecture of DLX was chosen based on observations about most frequently and used primitives in programs. DLX provides a good architectural model for study. DLX instructions can be classified into 4 classes. Name the classes and briefly describe each of them in your own words.

[8 marks]

b) There are 3 types of data hazards, which can be classified based on the order of read and write accesses in instructions. Name the three types of data hazard and illustrate them by consider two instructions, A and B. A occurs before B.



[9 marks]

c) Each of the classic scalar RISC designs fetched and tried to execute one instruction per cycle. The main common concept of each design was a five-stage execution instruction pipeline. During operation, each pipeline stage worked on one instruction at a time. Each of the stages consisted of an initial flip-flops and combination logic that operated on the outputs of the flip-flops. Explain in words and describe the instruction fetch (IF) cycle involved in DLX operation with the aid of diagram.

[6 marks]

d) Explain in your own words what is the meaning of Interleaved memory, and how it results to significantly higher memory throughput.

[2 marks]

Continued .....

Question 3

a) In computing, a vector processor or array processor is a central processing unit that implements an instruction set containing instructions that operate on one-dimensional arrays of data called vectors. Elaborate the FOUR properties of vector processing.

[6 marks]

b) RAM (Random Access Memory) is a kind of memory which needs constant power to retain the data in it, once the power supply is disrupted the data will be lost, and this is the main reason it is named as volatile memory. Briefly explain and differentiate between SRAM and DRAM in terms of mode of construction, speed, area of usage and power consumption.

[8 marks]

c) Given a bank busy time takes 6 clock cycles and a total memory latency is estimated to be 12 cycles, if we are given 8 memory banks:

i. Calculate the number of clock cycles required to complete a 64 element vector load with a stride of 1.

[3 marks]

ii. Estimate the number of clock cycles required to complete a 64 element vector load with a stride of 32

[3 marks]

d) Discuss how the sharing of branch predictors technique affects the branch activity and cause the increase of mispredictions for the long instruction sequences for actual programs.

[5 marks]

Continued .....

Question 4

a) Microcode is a computer hardware technique that interposes a layer of organisation between CPU hardware and the programmer-visible instruction set architecture of the computer. Microcode can be characterized as horizontal or vertical. Define the meaning of microcode and elaborate the differences between horizontal microcode and vertical microcode.

[6 marks]

b) In computing, a cache is a hardware or software component that stores data so that future requests for that data can be served faster, the data stored in cache might be the result of an earlier computation or a copy of data stored elsewhere. Elaborate and compare write-through cache and write-back cache in your own words.

[4 marks]

c) In a cache coherent multiprocessor, the caches provide both migration and replication of shared data items. Briefly describe what is migration and replication for enforcing coherence.

[2 marks]

d) A data-glow graph is a directed graph in which assignments and references to variables are represented by nodes, and information flow is represented by the arcs. Construct a data-flow graph for the following nested if-then-else statement.

```
if m > n then
        if j = p then
          z = c + d
        else
          z = e * f
else
        z = g + h
endif
```

[13 marks]

End of Paper